Circuit testing and fault simulation

Component
École Nationale Supérieure d'Électrotechnique d'Électronique

In brief

- **Ametys Code:** N9EE08B
- **Open to exchange students:** Yes

Presentation

Objectives

By the end of this course, students will be able to:
- Understand the destructive mechanisms affecting electronic circuits and the associated protection techniques.
- Master the fundamental concepts of integrated circuit reliability.
- Analyze and model faults in logic circuits and memories.
- Design and apply test generation strategies to detect faults in logic, sequential, and memory circuits.
- Implement design for test (DFT) methodologies to improve circuit testability.
- Explore advanced testing techniques for analog, mixed-signal, and RF circuits.
- Use simulation tools to evaluate the robustness and reliability of electronic circuits.

Description

1. Introduction
Presentation of the challenges of testing and fault simulation.
Importance of functional safety in modern integrated circuits.
2. Basic Concepts
Destructive mechanisms: wear, aging, physical failures.
Protection techniques: redundancy, circuit hardening.
Functional safety: reliability, availability, maintainability.
3. Logic circuit testing

Faults and patterns: classic faults (stuck-at, transition, delay, etc.), fault patterns.
Test generation: ATPG (Automatic Test Pattern Generation), fault coverage.
Sequential circuits: testing registers and automata.
Memory testing: specific failures, memory testing algorithms (March, BIST).
4. Design for Testability (DFT)
Principle: improving testability from the circuit design stage.
Generic techniques: scan chains, structured testability.
Built-in Test (BIT): principles and applications.
Built-in Self-Test (BIST): architectures and implementation.
5. Testing analog, mixed-signal, and RF circuits
Specific features: differences from digital circuit testing.
Test methods: parametric testing, functional testing.
DFT for analog and RF circuits: strategies and challenges.