Synthesis strategy

Component
École Nationale Supérieure d'Électrotechnique d'Électronique

In brief

- **Ametys Code:** N9EE05A
- **Open to exchange students:** Yes

Presentation

Objectives

By the end of this course, students will be able to:
- Understand the fundamental principles of microelectronics and the key stages in the manufacture of integrated circuits (analog, digital, mixed) and their applications.
- Master the fundamental concepts and structures of the VHDL language for hardware description.
- Write, simulate, and implement modules in VHDL, taking hardware constraints into account.
- Understand the direct link between code and hardware.
- Understand the concepts of timing, metastability, and asynchronism.
- Understand techniques for managing asynchronism.
- Design a test bench and perform simulations/debugging to verify circuit functionality.
- Perform circuit synthesis and routing, analyzing performance and optimizing architecture according to requirements.
- Understand power/performance/target trade-offs and digital circuit optimization strategies.

Description

Part 1: Overview of the world of microelectronics
Introduction to microelectronics
Basic principles and role in the electronics industry.
Historical evolution and technological advances.
Presentation of key materials and components

Wafers: manufacturing and role in circuit design.
Masks and packages: manufacturing processes and impact on performance.
Types of integrated circuits: analog, digital, mixed (examples and applications).
Presentation of basic VHDL structures and constraints.
Project presentation.
Part 2: Introduction to and in-depth study of the VHDL language
Practical work 1 – Introduction to basic structures (4 hours)
Understanding and modeling key components (RAM, ROM, DSP, etc.).
Use of generic structures (generics, constants, complex buses).
TP2 – Simulation and implementation (4 hours)
Creation and validation of a testbench.
Simulation and debugging of digital circuits.
Introduction to timing concepts (setup/hold) and associated constraints.
TP3 – Synthesis and optimization (4 hours)
Synthesis and routing processes on FPGA/ASIC.
Performance analysis and optimization strategies.
Power/performance/target trade-offs: partitioning, parallelization, resource sharing.
Part 3: Concepts of timing, metastability, and asynchronism
Practical work 4 – Timing, metastability, and asynchronism (4 hours)
Data flow constraints and asynchronism
Concepts of timing violations and metastability
Techniques for managing asynchronism