Analog ASIC project

Component
École Nationale Supérieure d'Électrotechnique d'Électronique

In brief

- **Ametys Code:** N9EE07B
- **Open to exchange students:** Yes

Presentation

Objectives

At the end of the analog integrated circuit design project, students will be able to structure and compose a sophisticated integrated circuit, demonstrating their mastery of the design stages when the specified performance of the integrated circuit is achieved.

Description

The project involves discovering, understanding, and mastering the various stages of designing a complex analog integrated circuit. In this context, Virtuoso® Schematic & Layout design tools are used to design a linear regulator including a bandgap voltage reference (5V/2V 10mA, BW >1MHz, PSRR 50dB) in sub-micron CMOS technology. After two lectures providing additional information to supplement the basic concepts acquired in L3 and M1, a project spread over N practical sessions will follow the design stages from the specifications to the drawing of the circuit masks using the Cadence® analog design flow environment. The main stages are: a bibliographic search of existing topologies, a design phase at the transistor level of the analog blocks that make up the circuit, a "worst-case" validation by parametric variation of the models of the components used, and the creation and design of the masks in accordance with the pairing rules.

The learning method used for this subject is Problem-Based Learning, which gives students a great deal of creative freedom when designing their circuits. Access to online documentation (open libraries, IEEE scientific articles, for example) provides the material needed to explore various circuit architectures that can meet the project's requirements.

Pre-requisites

Knowledge of the operating principles of bipolar and silicon MOSFET transistors (parameters, technology, MOSFET/BJT) as well as the basics of analog circuit design (common emitter/collector stage assembly, differential stage, push-pull circuit, etc.).