Microprocessor

Component
École Nationale Supérieure d'Électrotechnique d'Électronique d'Informatique d'Hydraulique et des Télécommunications

In brief

- **Ametys Code:** N7EE10C
- **Open to exchange students:** Yes

Presentation

Objectives

- Understand the **internal operation of a microprocessor and a microcontroller**.
- Distinguish fundamental concepts such as **sampling, quantization, resolution, memory organization, data buses, and instruction cycles**.
- Be able to **describe the architecture of a microcontroller**, particularly the **PIC families** (8-, 16-, and 32-bit).
- Learn how to **program a microcontroller** at a low level:
  - Understanding of **assembly language**,
  - Introduction to **C programming** for embedded systems.
- Be capable of **configuring and using internal peripherals** such as timers, ADCs, GPIO ports, UART, SPI, and interrupts.

Description

This course is a **comprehensive introduction to embedded microelectronics**.
It covers:

1. The **basic principles** of digital systems (sampling, quantization, buses, and memory).

2. The **detailed operation of a microprocessor**: arithmetic and control units, instruction cycles, and instruction sets.
3. **Memory types and hierarchy**: RAM, ROM, EEPROM, Flash, and their characteristics.
4. **PIC Microcontrollers**:

- **Harvard** vs **Von Neumann** architectures
- **RISC vs CISC** concepts
- Memory organization and **interrupt handling**
- On-chip peripherals: **I/O ports, timers, ADC, UART, SPI**, etc.
- Practical **assembly and C code examples** for PIC18 and PIC24.

The course combines **theory and hands-on practice**, focusing on understanding hardware architecture and low-level programming.

Pre-requisites

To follow this course effectively, students should have:

- Solid knowledge of **digital electronics** (bits, buses, binary logic).
- Basic understanding of **logic circuits and system architecture**.
- Some experience with **C programming** (variables, loops, syntax).
- An interest in **embedded systems** and **processor-level operation**.