Introduction to Cadence Layout XL / Spectrum

Component
École Nationale Supérieure d'Électrotechnique d'Électronique

In brief

- **Ametys Code:** N9EE06A
- **Open to exchange students:** Yes

Presentation

Objectives

Learn how to design the layout of an integrated circuit using design rules.

Learn how to use LVS verification tools.

Learn how to extract parasitic elements from a circuit.

Learn how to simulate the post-layout version of a circuit.

Learn how to analyze the comparison between the post-layout circuit and the ideal circuit.

Description

During this introductory course, participants will learn how to use the professional integrated circuit design software CADENCE with a CMOS operational amplifier in 0.35µm technology.

The layout must be designed in accordance with design rules. DRC/LVS verification tools and post-layout simulations that take into account mask-related parasitics are also covered.