

# FPGA system design for signal processing



Component  
École Nationale  
Supérieure  
d'Électrotechnique  
d'Électronique

## In brief

- > **Amety's Code:** N9EE08A
- > **Open to exchange students:** Yes

## Presentation

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### Objectives

Learn how to use a high-level synthesis tool to design signal processing functions for FPGAs.

Learn how to define and optimize a signal processing system architecture (TS function + interfaces and memory management).

Test and optimize the system on an FPGA board

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### Description

In this course, students take on the role of an engineer working for Thales Alenia Space, tasked with developing and implementing a spectrum analyzer on an FPGA. They must complete the following tasks:

- Analyze signal processing system architecture
  - Create IP using high-level synthesis in C++ (HLS)
  - Coding and synthesis of the architecture and IP in VHDL
  - Verification
  - Implementation on FPGA
  - Testing on board
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### Pre-requisites

Logic system design (UE N5EE03)

Digital electronics (UE N7EE08)

Digital systems architecture (N8EE03)