Synchronous design of digital systems

Component
École Nationale Supérieure d'Électrotechnique d'Électronique d'Informatique d'Hydraulique et des Télécommunications

In brief

- **Ametys Code:** N8EE03E
- **Open to exchange students:** Yes

Presentation

Objectives

- Understand the usefulness of synchronous digital circuits compared to asynchronous circuits (predictability, robustness against jitter and random events).
- Know and implement synchronous circuit design techniques.
- Know how to determine the essential parameters of such a circuit in order to understand its limitations (particularly time parameters).
- Be able to choose a circuit architecture to meet a constraint (operating frequency, size, power consumption).
- Design, on paper and in VHDL, state machines to describe the behaviour of digital circuits.

Description

The course consists of 5 hours and 15 minutes of lectures and 17 hours and 30 minutes of project work. It is assessed by means of a project report and the validation of milestones during the project sessions.

The lectures present the concepts described in the objectives from a theoretical perspective.

The project allows students to put these concepts into practice by designing a digital system in VHDL that uses a thermometer. Students must study the thermometer's datasheet to develop state machines that can communicate with this component.

Pre-requisites

- Knowledge of combinational and sequential electronics.
- Knowledge of low-level FPGA architecture as covered in the FPGA Technology course (N8EE03C)
- Proficiency in VHDL