

# ARCHITECTURE DES ORDINATEURS



In brief

> **Ametys Code:** N7EN07

## Presentation

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### Objectives

VHDL will be presented through examples of components. We will study its specific features (signals, parallel execution). Examples with increasing complexity will be considered, up to the design of the components of a computer (mini-processor, UART, memory hierarchy, ...). These components will be emulated on an FPGA. A project will consider a more complex example. In a second part, we will summarize the evolution towards multiprocessor architecture