Architecture and hardware acceleration for DL

Component
École Nationale Supérieure d'Électrotechnique d'Électronique d'Informatique d'Hydraulique et des Télécommunications

In brief

- **Ametys Code:** M34HOEV3
- **Open to exchange students:** Yes

Presentation

Objectives

This module provides an advanced methodology for designing elementary neural network functions using high-level synthesis (HLS) tools for optimal integration into an embedded system.